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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/051,679 | 01/16/2002 | Hasan Nejad | MI22-1877 | 1499 |

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| EXAMINER | |
|---|---|
| TRAN, LONG K | |
| ART UNIT | PAPER NUMBER |
| 2818 | |

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/051,679 | NEJAD, HASAN | |
| | Examiner | Art Unit | |
| | Long K. Tran | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 26 - 29* is/are rejected.

7)☒ Claim(s) *22-25 and 30-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of claims **1 – 33** in Paper No. **4** is acknowledged.

Claims **34 – 47** have been cancelled in Paper No. **4**.

Claims **1 – 33** are presented for examination.

### *Information Disclosure Statement*

2. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on January 16, 2002 and made of record as Paper No. **2**. The references cited on the PTOL 1449 form have been considered.

### *Specification*

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

a. The form and legal phraseology often used in patent claims, such as "means", "comprise" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

b. The examiner suggests to delete "; and Methods of Storing and Retrieving Information" from the title.

c. The disclosure is objected to because of the following informalities: in Brief Description Of The Drawings, Fig. 1 is cross-sectional view of an exemplary magnetoresistive memory device encompassed by the present invention; in paragraph 0033, Fig. 1 seems to be Prior art MRAM

Appropriate clarification is required.

4. The disclosure is objected to because of the following informalities: Specification, page 5, paragraphs 0013 and 0014: first electrically conductive line 14 and second electrically conductive 18. According to claims 1, 2, 7, 9, 12, 13, 14, 15, 22, 23, 25, 26, 28, 29 and 32, first conductive line should be 18 and second conductive line is 14 (first conductive line is in ohmic (physically) contacts one of the first and second magnetic layers of the stacks; second conductive line is spaced from the stacks).

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims **1**, **2**, **4**, **6**, **7 – 16, 18** and **26 – 29** are rejected under 35 U.S.C. 102(e) as being anticipated by Hosotani (US Patent Application Publication No. 2002/0037595).

Regarding claims **1, 2** and **6**, figures 1, 2 and 30A illustrate a magnetoresistive memory device, comprising: a memory bit comprising a stack 25 which includes a first magnetic layer 23, a second magnetic layer 24, and a non-magnetic layer 22 between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer; a first conductive line 27 proximate the stack and configured for utilization in reading information from the memory bit; and a second conductive line 29 spaced from the stack by a greater distance than any distance which the first conductive line is spaced from the stack, and configured for utilization in writing information to the memory bit; the first conductive line is in ohmic electrical contact with the magnetic layer 24 of the memory bit, and wherein the second conductive line is not in ohmic electrical contact with either of the magnetic layers of the memory bit; and the first conductive line physically contacts the first magnetic layer 24 (paragraphs 0006,0007, 0117 and 0121).

Regarding claim **4**, Hosotani discloses the non-magnetic layer 22 comprises an electrically insulation material (paragraph 0117).

Regarding claims **7** and **9**, Hosotani discloses an electrically insulation material 28 between the first and second conductive lines; and wherein the second conductive line is spaced from the stack by at least a combined thickness of the electrically

insulation material and the first conductive line; and the first conductive line 27 physically contacts the magnetic layer 24 (paragraph 0121).

Regarding claim **8**, Hosotani discloses the electrically insulation material 28 having a thickness of several tens to several hundreds angstroms; and as for insulating film, the dielectric layer 28 comprised silicon dioxide (paragraphs 0111 and 0077).

Regarding claims **10** and **11**, Hosotani discloses a third conductive line 20 proximate the stack; the third conductive line being configured for utilization in both writing information to the memory bit and reading information from the memory bit; and the first conductive line physically contacts one of the first and second magnetic layers, and wherein the third conductive line physically contacts the magnetic layer 23.

Regarding claim **12**, Hosotani discloses an electrically insulation material 28 between the first and second conductive lines; and wherein the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulation material and the first conductive line; the first conductive line 27 physically contacts the magnetic layer 24; and the third conductive line physically contacts the magnetic layer 23 (paragraph 0121).

Regarding claims**13** and **14**, Hosotani discloses a magnetoresistive memory device, comprising: a memory bit comprising a stack 25 which includes a first magnetic layer 23, a second magnetic layer 24, and a non-magnetic layer 22 between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer; a first conductive line 27 configured for utilization in reading information

from the memory bit in ohmic electrical contact with the magnetic layer 24; and a second conductive line 29 configured for utilization in writing information to the memory bit and not in ohmic electrical contact with either of the magnetic layers of the memory bit; and the first conductive line physically contacts one of the first and second magnetic layers (paragraphs 0006,0007, 0117 and 0121).

Regarding claims**15** and **16**, figures 1, 2 and 33 illustrate a magnetoresistive memory device, comprising: a stack 25 comprising a first magnetic layer 23, a second magnetic layer 24, and a non-magnetic layer 22 between the first and second magnetic layers; a first conductive line 27 over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; a second conductive line 20 under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; an electrically insulative spacer (not shown) under the second conductive line; and a third conductive line 13a under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; the first, second and third conductive lines alter a magnetic orientation within the same one of the two magnetic layers, and do not alter a magnetic orientation of the other of the two magnetic layers (paragraphs 0006,0007, 0149 – 0153)..

Regarding claim **18**, Hosotani discloses the non-magnetic layer 22 comprises an electrically insulation material (paragraph 0117).

Regarding claims **26, 28** and **29**, figures 1, 2 and 30A illustrate a magnetoresistive memory device assembly, comprising: an array comprising a plurality of individual memory bits; the memory bits including a stack 25 having a first magnetic layer 23, a second magnetic layer 24, and a non-magnetic layer 22 between the first and second magnetic layers; the memory bits storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer; a first conductive line extending across a first set comprising several of the individual memory bits of the array; the first conductive line being proximate the stacks of the first set of the individual memory bits of the array and configured for utilization in reading information from the memory bits; a second conductive line extending across the first set of the memory bits of the array and spaced from the stacks of the first set of the individual memory bits by a greater distance than any distance which the first conductive line is spaced from the stacks; the second conductive line being configured for utilization in writing information to the memory bits; a first transistor 62 electrically connected with the first set of the individual memory bits of the array through the first conductive line; and a second transistor 63 electrically connected with the first set of the individual memory bits of the array through the second conductive line; and an electrically insulation material 28 between the first and second conductive lines; wherein the second conductive line 29 is spaced from the stack by at least a combined thickness of the electrically insulation material and the first conductive

line; the first conductive line 27 physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits.(paragraphs 0006,0007, 0117 and 0121).

Regarding claim **27**, figure 2 illustrates the array 66 comprises a footprint over a supporting substrate, and wherein the first transistors 62 and second transistors 63 are peripheral to the footprint of the array.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims **3** and **5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani (US Patent Application Publication No. 2002/0037595) in view of Prinz (US Patent No. 6,381,170).

Regarding claims **3** and **5**, Hosotani disclosed the claimed invention of claim 1 except for the first and second magnetic layers comprise one or more of nickel, iron, cobalt, iridium, manganese, platinum and ruthenium; and the non-magnetic layer comprises an electrically conductive material.

It is conventional and also taught by Prinz that in a non-volatile random access memory employed GMR, typical material for ferromagnetic layers comprise nickel, iron

or cobalt (col. 5, lines 9 and 10; and col. 11, lines21 – 24); and for the non-magnetic layer comprises an electrically conductive material made of copper (col. 1, lines 59 – 63 and col. 11, lines 27 – 29).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use materials for the magnetic and non-magnetic layers as taught by Prinz into Hosotani's device in order to make a non-volatile random access memory employed GMR.

9. Claims **17, 20** and **21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani (US Patent Application Publication No. 2002/0037595) in view of Prinz (US Patent No. 6,381,170).

Regarding claims **17, 20** and **21**, Hosotani disclosed the claimed invention of claim 15 except for the first and second magnetic layers comprise one or more of nickel, iron, cobalt, iridium, manganese, platinum and ruthenium; and the non-magnetic layer comprises an electrically conductive material.

It is conventional and also taught by Prinz that in a non-volatile random access memory employed GMR, typical material for ferromagnetic layers comprise nickel, iron or cobalt (col. 5, lines 9 and 10; and col. 11, lines21 – 24); and for the non-magnetic layer comprises an electrically conductive material made of copper (col. 1, lines 59 – 63 and col. 11, lines 27 – 29).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use materials for the magnetic and non-magnetic layers as

taught by Prinz into Hosotani's device in order to make a non-volatile random access memory employed GMR.

10. Claim **19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hosotani (US Patent Application Publication No. 2002/0037595) in view of Koganei et al. (US Patent No. 6,055,179).

Regarding claim **19**, Hosotani disclosed the claimed invention of claim 15 except for the non-magnetic layer comprises aluminum oxide.

It is known and also taught by Koganei et al. (col. 19, lines 23 – 24 and 41 – 44) that non-magnetic layer is made of oxides or nitrides of Al, Si, Cu, Mg, etc. are used, among which aluminum oxides that have Fermi levels close to those of the other magnetic layers are more preferably used. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the non-magnetic layer made of aluminum oxides Hosotani's device in order to have layers in the stacks made of material having Fermi levels close to each other.

***Allowable Subject Matter***

11. Claims **22 – 25** and **30 – 33** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: Claims **22 – 25** and **30 – 33** allowable over the prior art of record because none of the prior art (Hosotani (US Patent Application Publication No. 2002/0037595), Prinz (US Patent No. 6,381,170) and Koganei et al. (US Patent No. 6,055,179)) whether

taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

a first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps (as claims 22 and 25); a second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp (as claims 23 and 25); and a third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps (as claims 24 and 25); the third conductive line proximate at least one memory bit of the first set of the individual memory bits; the third conductive line being configured for utilization in both writing information to the at least one memory bit and reading information from the at least one memory bit (as claim 30).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7466 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Long Tran LT

May 26, 2003

HOAI HO
PRIMARY EXAMINER